WHAT IS CLAIMED IS:

1. A semiconductor storage circuit comprising:

a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction;

data access circuit sections each of which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and includes a data access circuit for making data accesses to memory cells of one or more of said memory cell sub arrays belonging to said column and a first driver circuit for driving said data access circuit; and

a control circuit section for controlling said data access circuit through said first driver circuit,

wherein said data access circuit sections are disposed along the word line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are dispose along the word line direction.

2. The semiconductor storage circuit of Claim 1,

wherein the pitch at which said data access circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

3. The semiconductor storage circuit of Claim 1, further comprising:

power circuit sections each of which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and supplies a power voltage used in said semiconductor storage circuit; and

a power control circuit section for controlling a voltage supplying operation of

said power circuit sections,

wherein said power circuit sections are disposed along the word line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the word line direction.

4. The semiconductor storage circuit of Claim 3,

wherein the pitch at which said power circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

5. The semiconductor storage circuit of Claim 1, further comprising:

a row decoder circuit for selecting a word line of said memory cell array,

wherein each of said data access circuit sections includes a data line driver circuit for driving a data line of said memory cell array,

said control circuit section includes a second driver circuit and controls an operation of said row decoder circuit through said second driver circuit, and

said data line driver circuit and said second driver circuit are linearly arranged.

6. The semiconductor storage circuit of Claim 1,

wherein each of said memory cell sub arrays of said memory cell array includes a break area where placement of said memory cells is interrupted, and

said first driver circuit is disposed in each of said data access circuit sections in an area extending from said break area along the bit line direction.

7. The semiconductor storage circuit of Claim 6,

wherein said break area corresponds to a contact area of a strapping wire used for reducing resistance of a word line of each of said memory cell sub arrays of said memory cell array.

8. The semiconductor storage circuit of Claim 6,

wherein said break area corresponds to an area occupied by a sub word driver provided to each of said memory cell sub arrays of said memory cell array.

9. A semiconductor storage circuit comprising:

a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction;

row decoder sections each of which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and includes a row decoder circuit for selecting a word line of one or more of said memory cell sub arrays belonging to said row and a row decoder driver circuit for driving said row decoder circuit; and

a control circuit section for controlling an operation of said row decoder circuit through said row decoder driver circuit,

wherein said row decoder sections are disposed along the bit line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

10. The semiconductor storage circuit of Claim 9,

wherein the pitch at which said row decoder sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

11. The semiconductor storage circuit of Claim 9, further comprising:

power circuit sections each of which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and supplies a power voltage used in said semiconductor storage circuit; and

a power control circuit section for controlling a voltage supplying operation of said power circuit sections,

wherein said power circuit sections are disposed along the bit line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

12. The semiconductor storage circuit of Claim 11,

wherein the pitch at which said power circuit sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

13. The semiconductor storage circuit of Claim 9, further comprising:

a data access circuit for making data accesses to said memory cells of said memory cell array,

wherein each of said row decoder sections includes a word line driver circuit for driving a word line of said memory cell array selected by said row decoder circuit,

said control circuit section includes a third driver circuit and controls an operation of said data access circuit through said third driver circuit, and

said word line driver circuit and said third driver circuit are linearly arranged.

14. A semiconductor storage circuit comprising:

a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction;

data access circuit sections each of which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and includes a data access circuit for making data accesses to one or more of said memory cell sub arrays

belonging to said column and a first driver circuit for driving said data access circuit;

row decoder sections each of which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and includes a row decoder circuit for selecting a word line of one or more of said memory cell sub arrays belonging to said row and a row decoder driver circuit for driving said row decoder circuit; and

a control circuit section for controlling an operation of said data access circuit through said first driver circuit and controlling an operation of said row decoder circuit through said row decoder driver circuit;

wherein said data access circuit sections are disposed along the word line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are dispose along the word line direction, and

said row decoder sections are disposed along the bit line direction at a pitch equal to a pitch at which one or more of said memory cell arrays are disposed along the bit line direction.

15. The semiconductor storage circuit of Claim 14,

wherein the pitch at which said data access circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction, and

the pitch at which said row decoder sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit for increasing the storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

16. The semiconductor storage circuit of Claim 14, further comprising:

power circuit sections each of which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and supplies a power voltage used in said semiconductor storage circuit; and

a power control circuit section for controlling a voltage supplying operation of said power circuit sections,

wherein said power circuit sections are disposed along the word line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the word line direction.

17. The semiconductor storage circuit of Claim 16,

wherein the pitch at which said power circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

18. The semiconductor storage circuit of Claim 14, further comprising:

power circuit sections each of which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and supplies a power voltage used in said semiconductor storage circuit; and

a power control circuit section for controlling a voltage supplying operation of said power circuit sections,

wherein said power circuit sections are disposed along the bit line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

19. The semiconductor storage circuit of Claim 18,

wherein the pitch at which said power circuit sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit

used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

20. The semiconductor storage circuit of any of Claims 3, 11, 16 and 18,

wherein each of said power circuit sections includes at least one of a bit line precharge power circuit for supplying a precharging voltage for a bit line of said memory cell sub arrays and a word line power circuit for supplying an activating voltage for a word line of said memory cell sub arrays.

21. A layout method for a semiconductor storage circuit including a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction, comprising the steps of:

respectively generating layouts of said memory cell sub arrays and a data access circuit section which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and includes a data access circuit for making data accesses to said memory cells of one or more of said memory cell sub arrays belonging to said column and a first driver circuit for driving said data access circuit; and

repeatedly placing said memory cell sub arrays and said data access circuit section along the word line direction in such a manner that said data access circuit sections are disposed along the word line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are disposed along the word line direction.

22. The layout method for a semiconductor storage circuit of Claim 21,

wherein the pitch at which said data access circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

23. The layout method for a semiconductor storage circuit of Claim 21, further comprising the steps of:

generating a layout of a power circuit section which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and supplies a power voltage used in said semiconductor storage circuit; and

repeatedly placing said power circuit section along the word line direction in such a manner that said power circuit sections are disposed along the word line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the word line direction.

24. The layout method for a semiconductor storage circuit of Claim 23,

wherein the pitch at which said power circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

25. The layout method for a semiconductor storage circuit of Claim 21, further comprising the steps of:

generating a layout of a control circuit section that has a second driver circuit and controls an operation of a row decoder circuit for selecting a word line of said memory cell array through said second driver circuit; and

placing said control circuit section to be arranged along the word line direction together with said data access circuit sections,

wherein each of said data access circuit sections includes a data line driver circuit for driving a data line of said memory cell array, and

said data line driver circuit and said second driver circuit are linearly arranged.

26. The layout method for a semiconductor storage circuit of Claim 25,

wherein lengths along the bit line direction of circuit areas of said data line driver circuit and said second driver circuit are increased or reduced in accordance with increase or reduction of storage capacity of said semiconductor storage circuit performed by increasing or reducing a number of said memory cell sub arrays arranged along the bit line direction.

27. A layout method for a semiconductor storage circuit including a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction, comprising the steps of:

respectively generating layouts of said memory cell sub arrays and a row decoder section which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and includes a row decoder circuit for selecting a word line of one or more of said memory cell sub arrays belonging to said row and a row decoder driver circuit for driving said row decoder circuit; and

repeatedly placing said memory cell sub arrays and said row decoder section along the bit line direction in such a manner that said row decoder sections are disposed along the bit line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

28. The layout method for a semiconductor storage circuit of Claim 27,

wherein the pitch at which said row decoder sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

29. The layout method for a semiconductor storage circuit of Claim 27, further comprising the steps of:

generating a layout of a power circuit section which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and supplies a power voltage used in said semiconductor storage circuit; and

repeatedly placing said power circuit section along the bit line direction in such a manner that said power circuit sections are disposed along the bit line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

30. The layout method for a semiconductor storage circuit of Claim 29,

wherein the pitch at which said power circuit sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

31. The layout method for a semiconductor storage circuit of Claim 27, further comprising the steps of:

generating a layout of a control circuit section that has a third driver circuit and controls an operation of a data access circuit for making data accesses to said memory cells of said memory cell array through said third driver circuit; and

placing said control circuit section to be arranged along the bit line direction together with said row decoder sections,

wherein said row decoder section includes a word line driver circuit for driving a word line of said memory cell array selected by said row decoder circuit, and

said word line driver circuit and said third driver circuit are linearly arranged.

32. The layout method for a semiconductor storage circuit of Claim 31,

wherein lengths along the word line direction of circuit areas of said word line driver circuit and said third driver circuit are increased or reduced in accordance with

increase or reduction of storage capacity of said semiconductor storage circuit performed by increasing or reducing a number of said memory cell sub arrays arranged along the word line direction.

33. A layout method for a semiconductor storage circuit including a memory cell array in which memory cell sub arrays each including a plurality of memory cells are arranged in an array along a bit line direction corresponding to a column direction and a word line direction corresponding to a row direction, comprising the steps of:

respectively generating layouts of said memory cell sub arrays, a data access circuit section which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and includes a data access circuit for making data accesses to said memory cells of one or more of said memory cell sub arrays belonging to said column and a first driver circuit for driving said data access circuit, and a row decoder section which is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and includes a row decoder circuit for selecting a word line of one or more of said memory cell sub arrays belonging to said row and a row decoder driver circuit for driving said row decoder circuit; and

repeatedly placing said memory cell sub arrays and said data access circuit section along the word line direction in such a manner that said data access circuit sections are disposed along the word line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are disposed along the word line direction and repeatedly placing said memory cell sub arrays and said row decoder section along the bit line direction in such a manner that said row decoder sections are disposed along the bit line direction at a pitch equal to a pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

34. The layout method for a semiconductor storage circuit of Claim 33,

wherein the pitch at which said data access circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction, and

the pitch at which said row decoder sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing the storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.

35. The layout method for a semiconductor storage circuit of Claim 33, further comprising the steps of:

generating a layout of a power circuit section which is provided correspondingly to a column of said memory cell sub arrays arranged along the bit line direction and supplies a power voltage used in said semiconductor storage circuit; and

repeatedly placing said power circuit section along the word line direction in such a manner that said power circuit sections are disposed along the word line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the word line direction.

36. The layout method for a semiconductor storage circuit of Claim 35,

wherein the pitch at which said power circuit sections are disposed along the word line direction corresponds to a length along the word line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the word line direction.

37. The layout method for a semiconductor storage circuit of Claim 33, further comprising the steps of:

generating a layout of a power circuit section that is provided correspondingly to a row of said memory cell sub arrays arranged along the word line direction and supplies a power voltage used in said semiconductor storage circuit; and

repeatedly placing said power circuit section along the bit line direction in such a manner that said power circuit sections are disposed along the bit line direction at a pitch equal to the pitch at which one or more of said memory cell sub arrays are disposed along the bit line direction.

38. The layout method for a semiconductor storage circuit of Claim 37,

wherein the pitch at which said power circuit sections are disposed along the bit line direction corresponds to a length along the bit line direction of a circuit extension unit used for increasing storage capacity of said semiconductor storage circuit by increasing a number of said memory cell sub arrays arranged along the bit line direction.